ABSTRACT

Level-shifting circuitry having a level-shifting section responsive to an input logic signal. The input logic signal has a first voltage level representative of a first logic state or a second voltage level representative of a second logic state. The level-shifting section provides an output logic signal at an output terminal having a third voltage level representative of the first logic state of the input logic signal. The level-shifting circuitry also includes an enable/disable section responsive to an enable/disable signal for placing the output terminal at a relatively high output impedance condition independent of the logic state of the input signal during a disable mode. The level-shifting section includes: an input transistor having a control electrode, a first electrode coupled to the input logic signal, and a second electrode. An output pair of serially coupled complementary type transistors is provided. A first one of the pair of transistors has a first electrode coupled to a source of the third voltage level through a first switching transistor and a control electrode coupled to the second electrode of the input transistor. A junction between the output pair of transistors provides an output terminal for the level-shifting circuitry. A control electrode of the second one of the pair of transistors is connected to the first electrode of the input transistor. The second one of the pair of transistors has a second electrode coupled to the second voltage level through a second switching transistor. The first and second switching transistors are fed by the enable/disable signal. The level-shifting section includes an additional transistor. The additional transistor has a control electrode connected to the junction, a first electrode coupled to the source of the third voltage level through the first switching transistor and a second electrode connected to the second electrode of the input transistor. The input transistor and the additional transistor are of opposite conductivity type. The enable/disable circuit includes an inverter fed by the enable/disable signal, such inverter having an output coupled to the control electrode of the first switching transistor. The inverter is powered by a source of the first voltage level, in which case, the inverter comprises a level shifter for shifting the level of the enable/disable signal from the first voltage level to the third voltage level and for feeding such third voltage level to the control electrode of the first switching

transistor to placing the first switching transistor to a non-conducting condition during the disable mode.